CLAIMS

What is claimed is:

1. A multi-chip module instrument controller comprising:

a non-volatile memory storage component for program and data storage;

a large volatile memory storage component for additional program and data storage;

a processor coupled to both said non-volatile memory storage component and said large volatile memory storage components, said processor capable of high-frequency and low-frequency operations and having an embedded memory for storing an initialization program that enables the processor to start up processing without first retrieving a program from the non-volatile memory;

at least two internal oscillators coupled to the processor, for providing clock signals for the low-frequency and high-frequency operations;

a plurality of gates arranged in a field programmable gate array, said gate array coupled to said processor and configured to run independent processes in parallel with said processor; and

a plurality of analog-to-digital converters for receiving a plurality of analog inputs, digitizing said analog inputs at one of at least two possible bit depths, thereby generating digital inputs, and providing said digital inputs to said processor.

2. The multi-chip module instrument controller of claim 1, further comprising a plurality of analog outputs, each output being controlled by an independent digital-to-analog converter, each of said independent digital-to-analog converters being configured to convert from one of at least two possible depths to analog.

3. The multi-chip module instrument controller of claim 1, wherein:

a first portion of the gates in the field programmable gate array is configured to perform signal processing; and

a second portion of the gates in the field programmable gate array is configured to operate as a signal distribution matrix for rerouting signals within the multi-chip module instrument controller.

4. The multi-chip module instrument controller of claim 1, wherein the microprocessor includes an embedded memory that enables the startup of processing without first loading a program from the non-volatile memory.

5. The multi-chip module instrument controller of claim 1, further comprising a resettable digital real-time quartz controlled clock for accurate date and time stamping of data before it is stored in the non-volatile memory.

6. The multi-chip module instrument controller of claim 5, wherein a portion of the gates in the field programmable gate array are configured to operate as an internal embedded power converter capable of receiving an input voltage level and generating each operating and reference voltage needed within the instrument controller.

7. A multi-chip module instrument controller comprising:

a processor configured to automatically activate from a totally deactivated (unpowered) state upon receiving an external activation signal, perform proscribed operations, and automatically return to a totally deactivated state using no power; and

a plurality of gates arranged in a field programmable gate array, said gate array coupled to said processor and configured to run independent processes in parallel with said processor.

8. The multi-chip module instrument controller of claim 7, further comprising:

a non-volatile memory storage component coupled to said processor for program and data storage;

at least two internal oscillators coupled to the processor for providing clock signals for low-frequency and high-frequency operations;

a plurality of analog-to-digital converters for receiving a plurality of analog inputs, digitizing said analog inputs at one of at least two possible bit depths, thereby generating digital inputs, and providing said digital inputs to said processor.

9. The multi-chip module instrument controller of claim 8, further comprising a plurality of analog outputs each output being controlled by an independent digital-to-analog converter, each of said independent digital-to-analog converters being configured to convert from one of at least two possible bit depths to analog.

10. The multi-chip module instrument controller of claim 8, wherein a portion of the gates in the field programmable gate array is configured to operate as an

internal embedded power converter capable of receiving an input voltage level and generating each operating and reference voltage needed within the instrument controller.

11. A method for conducting multiple parallel signal processing using a single multi-chip module instrument controller having a processor and a field programmable array, said method comprising:

receiving a plurality of analog inputs, digitizing said analog inputs at one of at least two possible bit depths (thereby generating digital inputs),

providing a first portion of said digital inputs to said processor,

providing a remaining portion of said digital inputs to said field programmable gate array;

performing digital signal processing on said first portion of said digital inputs utilizing the processor; and

receiving the remaining portion of the digital inputs at the field programmable gate array and configuring a first portion of the gates in the field programmable gate array to perform digital signal processing on the remaining portion of said digital inputs, thereby conducting multiple parallel signal processing using a single multi-chip module instrument controller.

12. The method for conducting multiple parallel monitoring and control functions using a single multi-chip module instrument controller as in claim 11, further comprising the additional step of providing at least two internal oscillator signals to the processor for low-speed and high-speed digital signal processing operations.

13. The method for conducting multiple parallel monitoring and control functions using a single multi-chip module instrument controller as in claim 11, further comprising the step of configuring a section portion of the gates in the field programmable gate array to operate as an internal embedded power converter capable of receiving an input voltage level and generating each operating and reference voltage needed within the instrument controller.